**REMARKS**

This is in response to the Official Action currently outstanding with respect to the above-identified application, which Official Action the Examiner has designated as being a FINAL Official Action.

Claims 1-20 are pending, but Claims 3, 6, 9 and 14-18 have been withdrawn from further consideration as being directed to a non-elected invention and species, the election having been made without traverse. By the foregoing Amendment, Claims 1, 2, 4, 5, 11, 12, 19 and 20 have been amended for purposes of clarifying the expression of inherent features already present therein. No Claims have been canceled and no Claims have been added. Accordingly, in the event that the Examiner grants entry to the foregoing Amendment, Claims 1, 2, 4, 5, 7, 8, 10-13, 19 and 20 will constitute the claims under active prosecution in this application.

The foregoing Amendment sets forth the claims of this application as they will stand in the event that the Examiner grants entry to this Amendment After Final Rejection Under 37 CFR 1.116 as required by the Rules.

In the currently outstanding Official Action, the Examiner has:

1. Acknowledged Applicant's claim for foreign priority under 35 USC 119(a)-(d) or (f), and confirmed the receipt by the United States Patent and Trademark Office of the required certified copy of the priority document;

2. Indicated that the drawings filed on 20 October 2000 have been accepted, and that the drawing changes proposed with Applicants' previous Amendment of 16 April 2003 have been approved, and required Applicants to submit new formal drawings incorporating the approved changes;

3. Acknowledged Applicants' Information Disclosure Statement of 13 January 2003 by providing Applicants with a copy of the Form PTO-1449 that accompanied that submission duly signed, dated and initialed by the Examiner in confirmation of his consideration of the art listed therein;

4. Rejected Claim 20 under 35 USC 112, first paragraph as failing to comply with the written description requirement.

5. Rejected Claims 1, 4, 7, 10, 19 and 20 under 35 USC 102(b) as being anticipated by the Takeda, et al reference (US Patent No. 5,398,043).

6. Rejected Claim 20 as being anticipated by "Applicants' Admitted Prior Art" under 35 USC 102(b);

7. Rejected Claims 2, 5, 8, and 11-13 under 35 USC 103(a) as being unpatentable over the Takeda, et al reference;

8. Indicated that Applicants' arguments of 16 April 2003 have been considered but are not deemed to be persuasive on the grounds that he believes that the Takeda reference teaches supplementary capacitive drive circuitry that maintains a predetermined potential difference between supplementary capacitance lines and common signal lines.

Further comment regarding items 1 and 3 above is not deemed to be required in these Remarks.

With respect to item 2, Applicants are submitting concurrently herewith a new set of formal drawings for this application that incorporate the drawing changes approved by the Examiner. It is respectfully submitted that this submission fully complies with the Examiner's outstanding requirements concerning the drawings of this application.

With respect to items 4 and 6, Applicants respectfully call the Examiner's attention to the foregoing Amendment wherein the wording of Claim 20 has been amended so as to indicate that the supplemental drive circuit includes: "a reference input maintained at the same potential as that of the common electrode for driving the supplemental capacitance lines so that a predetermined potential difference between the voltage applied to the counter electrode and the voltages applied to the pixel electrodes is always maintained when any of the pixel electrodes and supplemental capacitances leaks."

The Examiner's comments in the currently outstanding FINAL Official Action suggest that he feels that the previous wording of Claim 20 to the effect that the voltage applied to the counter electrode is applied to the supplementary capacitance drive circuit is contrary to the teachings of the present invention to the effect that "the supplementary capacitance lines 23 are driven by a supplementary capacitance drive circuit independently of the common signal lines 26" as stated at page 24, first paragraph of the present specification. Applicants respectfully submit that this application is not, and was never intended to be, limited in the manner suggested by the Examiner.

In support of this assertion, Applicants respectfully direct the Examiner's attention to Figure 1 of the present application wherein it is clearly shown that the potential level of line 26 (the counter electrode potential) is contemplated in the embodiment therein shown to be an input to circuit 27 (the supplementary capacitance drive circuit). This concept is explained at Page 26 of the present specification to the effect that the circuit 27 is to drive the supplemental capacitance so that a predetermined potential difference is maintained between the pixel electrodes and the counter electrode. One way that this is accomplished is to utilize the potential of line 26 as a reference input to circuit 27 while circuit 27 otherwise acts independently.

Of course, the same result could be achieved by any reference signal having the same potential as that of the Com signal. The important point, however, is that a potential having a fixed (predetermined) difference from that of the Com line is applied to the supplemental capacitance and that that signal changes along with changes in the Com signal that drives the Com signal lines so as to maintain the predetermined potential difference called for in the claims (see the present specification at page 25, line 17 to page 26, line 17).

Accordingly, Applicants respectfully submit that the Examiner's rejection of Claim 20 under 35 USC 112, first paragraph, it without merit and should be withdrawn.

Similarly, Applicants respectfully submit that the Examiner's rejection of Claim 20 under 35 USC 102(b) as being anticipated by "Applicants' Admitted Prior Art" also is without merit. The prior art referred to in Applicant's specification is that shown in Fig. 8. One of the configurations contemplated by Claim 20 is that shown in Fig. 1. A comparison of Fig.8 with Fig. 1 reveals that in Fig. 8 both the Com line and the supplemental capacitance line are at the same potential. Fig. 1, on the other hand, simply shows the potential of the Com line as **one of the multiple inputs** to the capacitance drive circuit 27. Hence, the circuit 27 specifically is shown as having inputs other than that from the Com line, and the wording of Claim 20 immediately prior to the wording objected to by the Examiner precludes the construction admitted as being prior art in the present specification being the same as the structure claimed by Claim 20.

Accordingly, while Applicants have elected to refine the wording of Claim 20 by the foregoing amendment so as to broaden it and clarify that it is to cover any source of reference potential representative of the Com line potential relative to which the supplemental capacitance line potential is to be varied, the fact remains that as previously worded Claim 20 was both supported by the present specification as originally filed (see particularly Fig. 1 and pages 25-26) and not anticipated by the prior art circuitry of Fig. 8 described in the background portion of the specification. Hence, Applicant respectfully submits that the outstanding rejections of Claim 20 under 35 USC 112 and under 35 USC 102(b) as they relate to the teachings and disclosures of the present specification are in error and should be withdrawn. Further, Applicants respectfully submit that Claim 20 as hereinabove amended clarifies the distinctions just discussed and should be granted entry for that reason. Therefore, reconsideration and withdrawal of the outstanding rejections of Claim 20 based upon the wording of the present specification are respectfully requested in response to this communication.

The Examiner's remaining rejections stand or fall on the basis of his statement to the effect that the Takeda et al reference includes a supplementary capacitance drive circuit for driving the supplemental capacitance lines so that ***a predetermined potential difference from the voltage applied to counter electrode always is maintained*** when any of the pixel electrodes and supplementary capacitance lines leaks.

As mentioned previously, the Takeda, et al reference discloses a method for driving an active-matrix liquid crystal display device with an A.C. power supply to improve display quality, driving reliability and reduce power consumption by removing the majority of the adverse effects of D.C voltages generated in the display device due to the dielectric anisotropy of the liquid crystal and the parasitic capacitances of the TFT/pixel electrode. To accomplish this, a scan signal Vg is applied to the scan signal wiring 1, an image signal Vs is applied to the image signal wiring 2, a modulation signals Ve (Ve(-), Ve(+)) are applied to one electrode of the storage capacitance Cs in accordance with the image signal having its polarity inverted every field, and a constant counter voltage Vt is applied to the counter electrode of the liquid crystal capacitance Clc* for each field.

The result of this is that when the TFT is in its off state, the potential of the pixel electrode is in a floating condition and the influences of the driving voltages appear on the pixel electrode. Further, when the compensation voltages Ve(+) and Ve(-) are ideally set, the scan signal Vg (that includes such offsets or superimpositions of the compensation voltages as may be present) negates the D.C. potential induced between the image signal wiring and the pixel electrode by way of the parasitic capacitance Cgd 4 so that the value of the D.C. potential is made to be zero. Hence, in the Takeda, et al ideal case, a signal is supplied having an inverted polarity at every field with respect to the potential of the counter electrode with the overall effect that no D.C. potential attributable to the parasitic capacitance of the TFT/pixel or the dielectric anisotropy of the liquid crystal is present between the pixel and the counter electrode across the liquid crystal.

In Takeda, et al, however, "(t)he amount of potential change of the modulation signal Ve(+) in the positive direction and that Ve(-) in the negative direction are made independently variable." See, Column 10, lines 40-45. This feature is important to Takeda et al because the goal of the invention of that patent is to avoid the problems in "capacitive-coupled drives" arising from the fact that gate signal delays cause charging errors in the transmission of source signals to the pixel electrode within the allowed gate ON time periods and/or time delays in gate voltages reaching their OFF levels resulting in leakage and changes in pixel potential. These problems are not solved by the expedient of varying TFT channel width and channel length due to parasitic capacitance problems such variations cause. Thus, Takeda et al resort to the utilization of one or more preliminary gate ON signals followed by a substantial gate ON signal in order to effectively charge their pixels within the allowed gate ON periods. According to Takeda et al this is best accomplished by bringing the nth pixel potential to the level of the (n-2)th pixel potential (i.e., that of the last field of the same type) and thereafter utilizing the correction voltages Ve to charge the pixel to its ultimately desired level during the so-called substantial gate ON period.

Takeda et al do this by initiating the preliminary gate ON periods prior to the shift from the preceding period and setting the modularization voltages preliminarily before the end of the preliminary gate ON signal. If this is attempted later, the jump from the preliminary level turns out to exceed the jump from a level equivalent to that to the next preceding field of the type being charged thereby rendering the preliminary charging useless. As a result, as shown in Fig. 2(d) of the Takeda et al reference, Ve(+) is set as the initial drop at Gate ON at T1 and Ve(-) is set as the difference between the lowest level at gate ON at T1and zero. (See, Takeda, et al at Column 9, lines 12-58)

The important point, however, remains that as mentioned the values for Ve(+) and Ve(-) are ***independently variable*** according to the situation, and Takeda et al does not teach, disclose or suggest that a ***predetermined potential difference would always be maintained between the pixel electrodes and to counter electrode if the pixel capacitance or supplemental capacitances taught therein were to leak***. Nothing in the Takeda et al reference associates variations in the voltage applied to the counter electrode with either Ve(+) or Ve(-). Indeed, the potential of the counter electrode is always held constant in the Takeda et al. reference, while the correction voltages Ve(+) and Ve(-) applied via the supplemental capacitance are superimposed on or offset the scan signal, and are adjustable to do so equally, or as close to equally as possible, so as to avoid the inducement of DC effects.

The present invention, on the other hand, is different. It is directed to the maintenance of a ***predetermined potential difference between the counter electrode and the pixel electrodes*** by the provision of a supplementary capacitance that assures that any potential leakage from the supplementary capacitance or the parasitic capacitance of the TFT/pixel electrodes is compensated at least to the predetermined potential difference level. Hence, a capacitance leakage either in the supplemental holding capacitor or in the parasitic capacitance associated with the TFT/pixel cannot cause the potential difference between the counter electrode and the pixel electrodes to reach a level wherein bright spots and the like damage the image.

In summary, therefore, the cited Takeda et al reference is not concerned with and does not teach, disclose or suggest, that the potential difference between the pixel electrode and the counter electrode must always be maintained at a no less than a predetermined level such that bright spots will not damage the image. Takeda, et al rather has the goal of driving the display device with an AC power supply in a manner that compensates for the limitation on the charging of the device occasioned by the permitted gate ON period.

Accordingly, while it may be true that if the pixel capacitance or the supplemental capacitance in the Takeda et al reference structure leaks some level of potential difference between the pixel electrode and the counter electrode will be maintained, there is clearly and definitely nothing in the Takeda et al reference that teaches, discloses or suggests that a **predetermined potential level will always be so maintained**. In Takeda et al both Ve(+) and Ve(-) are individually adjustable with the emphasis being upon adjustments that will result in the overall DC potential being made to be zero, or as close to zero as possible. Accordingly, nothing in the Takeda, et al reference is sufficient to render the present invention either anticipated or obvious to one skilled in the art as of the time that it was made.

Accordingly, Applicants respectfully submit that previously pending claims 1-2, 4, 5, 7, 8, 10-13, 19 and 20 are allowable over the art currently of record, and that the Examiner's presently outstanding rejections should be withdrawn. A decision so holding and allowing all of the claims of this application is respectfully requested in response to this communication. Alternatively, in the event that the Examiner still refuses allowance, entry of the foregoing amendment for purposes of Appeal is respectfully requested.

For each and all of the foregoing reasons, reconsideration and allowance of the present application is respectfully requested.

Applicants believe that additional fees are not required in connection with the consideration of this response to the currently outstanding Official Action. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge and/or credit Deposit Account No. **04-1105**, as necessary, for the correct payment of all fees which may be due in connection with the filing and consideration of this communication.

Respectfully submitted,

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